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PRESTOR-1: A Processor Extending Multithreaded Architecture

Tanaka, K.
Japan Advanced Institute of Science and Technology

This paper appears in: **Innovative Architecture for Future Generation High-Performance Processors and Systems, 2005**

Publication Date: 17-19 Jan. 2005

On page(s): 91 - 98

ISSN: 1527-1366

Digital Object Identifier: 10.1109/MWA.2005.39

Posted online: 2006-02-06 08:53:50.0

Abstract

Multithreaded processors are globally spreading. Multithreaded architecture enables fast context switching for tolerating memory access latency and bridging synchronization gap, and thus enables efficient utilization of execution pipelines. However, it cannot avoid all pipeline stalls; stalls will still occur when all processor built-in threads are in a wait state or there are not enough threads in a task/process to fill up all available context slots, since the mechanism for switching active threads is effective only for processor built-in threads' contexts. We developed a new multithreaded processor, PRESTOR-1, that increases the virtual number of built-in threads' contexts and enables seamless task/thread switching by allocating and swapping task/thread contexts hierarchically between processor and memory in a multitasking environment. The processor supports real-time applications through hierarchical task/thread allocation based on the task/thread priority and fast response mechanisms for **interrupt requests** exploiting the multiple-context architecture. Moreover, the processor has reconfigurable caches that provide a priority-based partitioning cache and an FIFO buffer. In this paper, we describe the details of PRESTOR-1.

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